Considerations for Embedding Passives and Actives in PCBs

PwrSoC 2014

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Agenda

- Why embedding?
- Embedding flavours
- Embedding by AT&S
- Reliability comparison
- Supply chain
- Comparison with QFN
- Conclusion

What is embedding?

Styles

- Layer embedding

⇨ Capacitive and/or resistive layers

- Partial embedding

⇨ Cavities in substrates

- Full embedding

⇨ Components in substrates

⇨ Focus on ECP from AT&S

Why are we embedding?

Trends and challenges in electronics

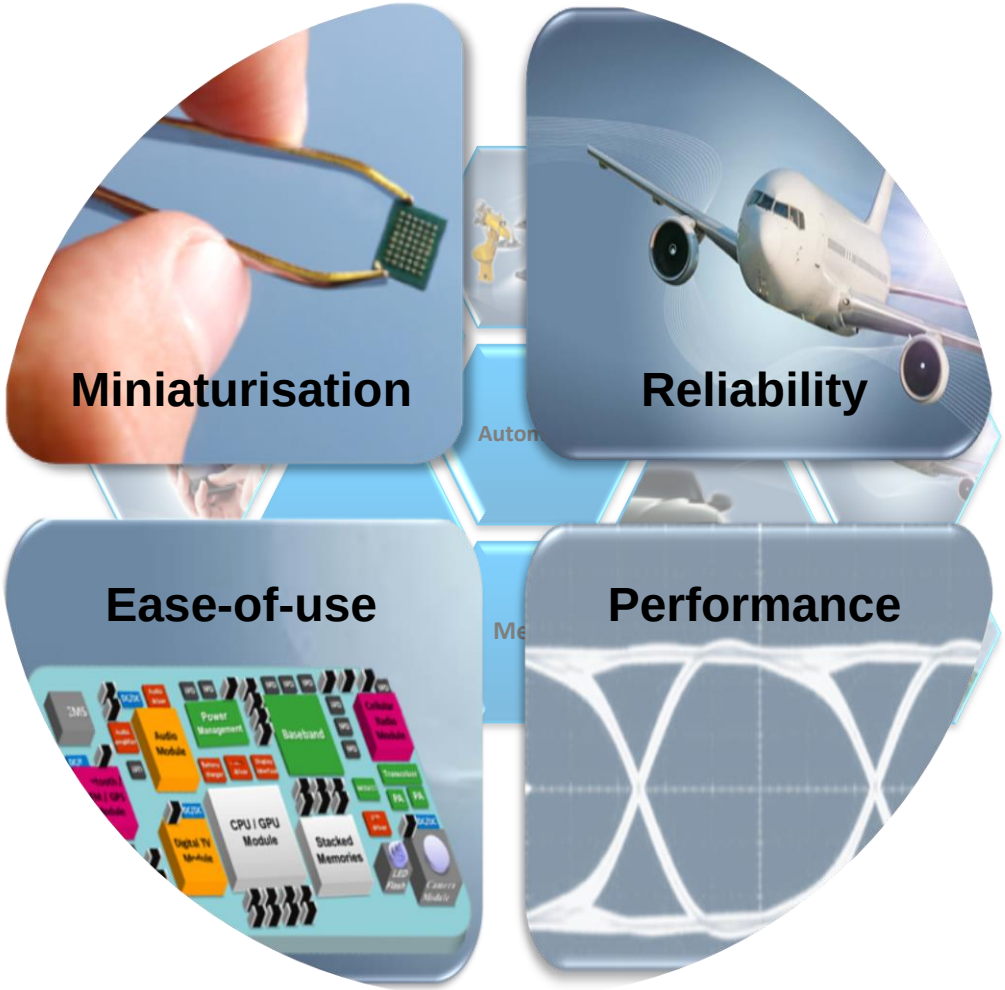
More functions

Smaller devices

Shorter development cycles

Increased component density

More-fragile components



More-complex supply-chain

Increased cost of IC design

Higher power dissipation

Lower power

Increased clock frequency

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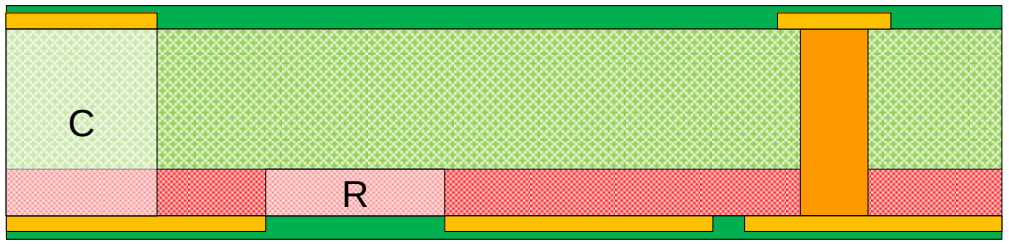
Embedding flavours

Embedded layer

- Pros
  - High flexibility in number and position of passive functions
  - General compatibility with standard PCB processes

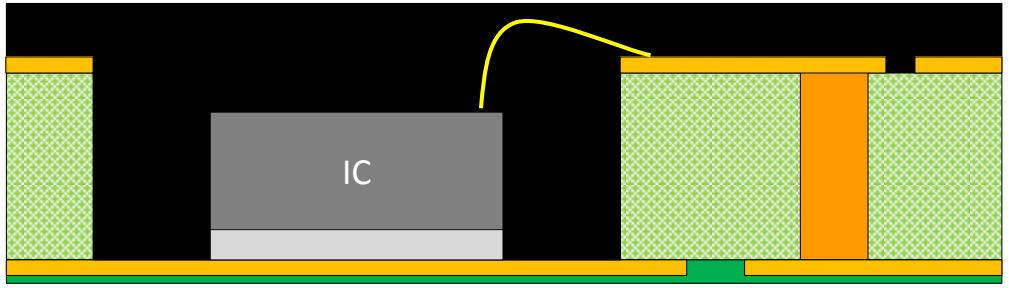
- Cons
  - Higher material cost than standard PCB
  - Limitation to low passive values
  - Limitation to passive functions



Embedding flavours

Partial embedding

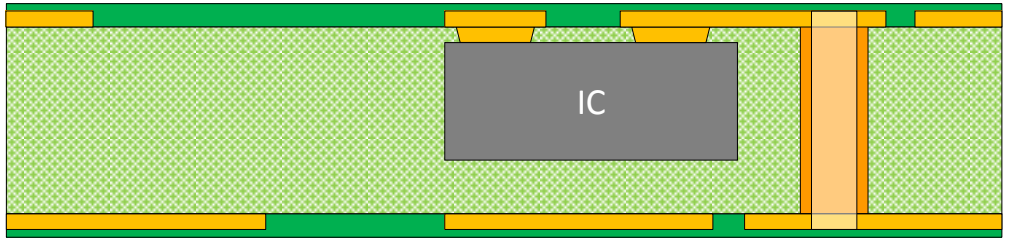
- Pros
  - Similar price to standard PCB
  - Compatibility with standard components
  - Possibility to improve electrical/thermal performance
- Cons
  - Increased complexity of component placement
  - Loss of integration
  - Limitation to wirebonded actives for low-layer-count PCBs



Embedding flavours

Full embedding

- Pros
  - Miniaturisation through 3D integration
  - Increased performance through short connections
  - Increased performance through heat conduction
- Cons
  - Higher m2 price
  - Limitation to process-compatible components



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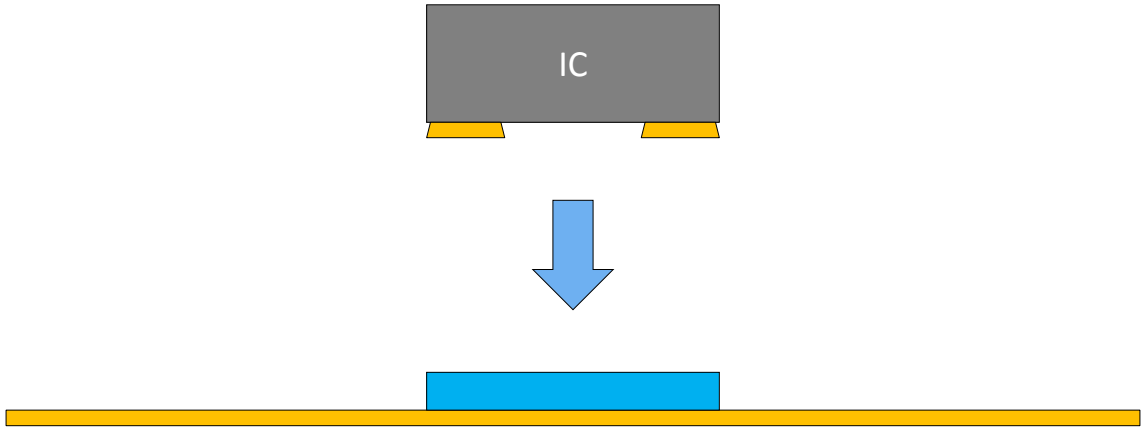
Embedding by AT&S

Component placement



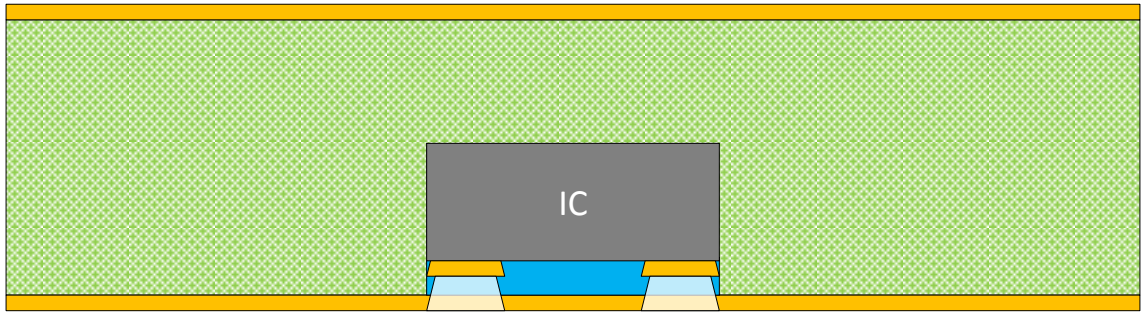
Embedding by AT&S

Component placement

- 1 ASM X4 equivalent to 80 die placers

Embedding by AT&S

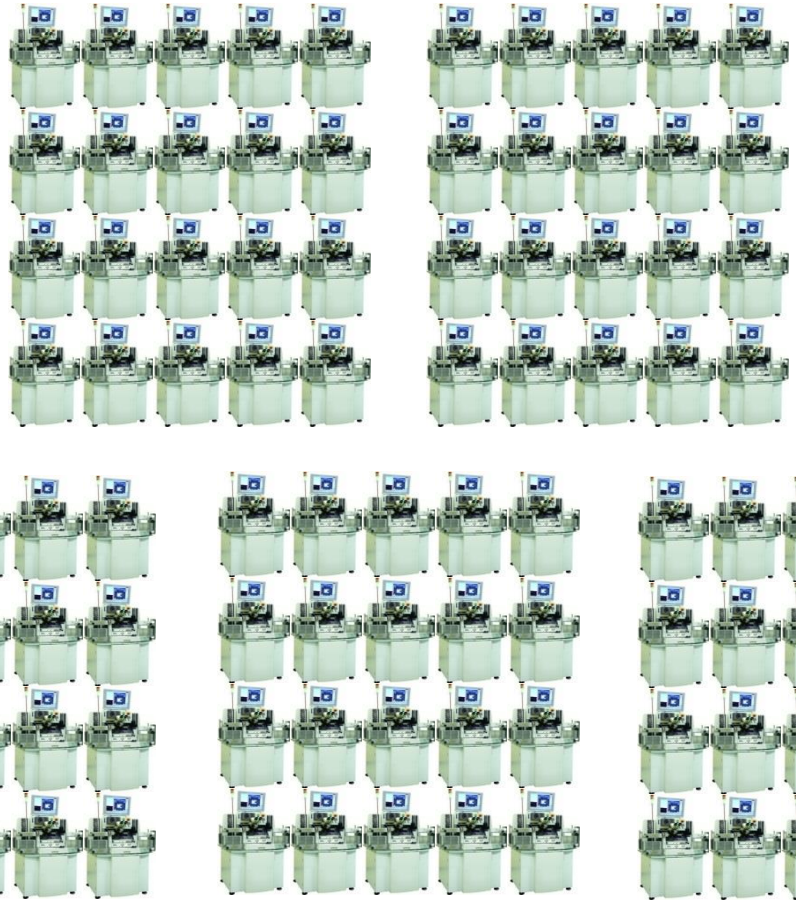
PCB and interconnect formation



Embedding by AT&S

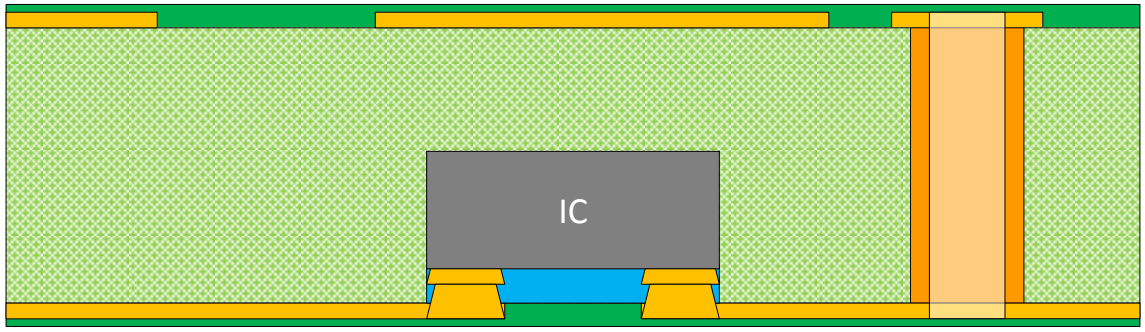
Interconnect formation

- 1 laser-drilling station equivalent to 100 wirebonders



Embedding by AT&S

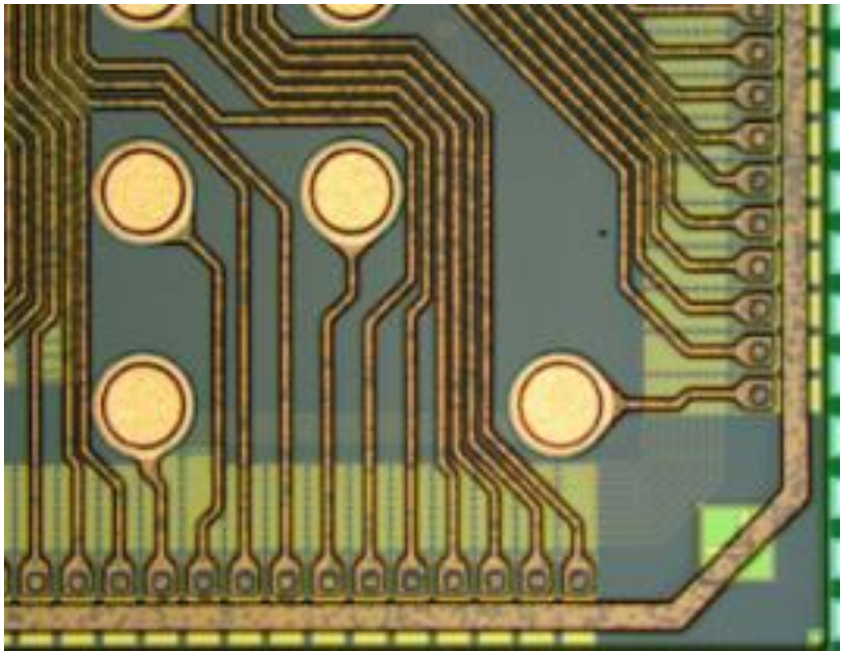
Structuring and finish

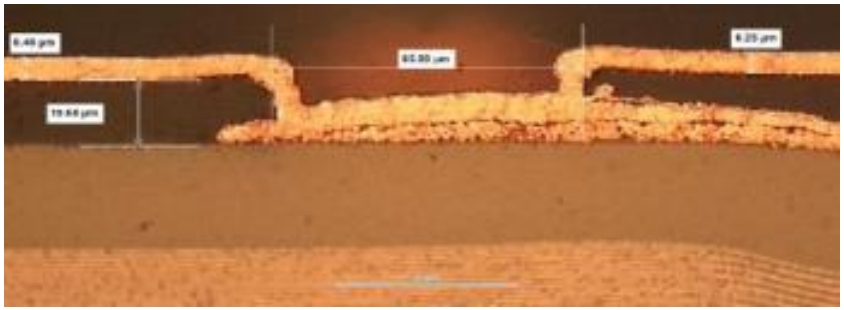


Embedding by AT&S

Requirements

- Cu terminations (minimum 5 mm)
- Components in tape-&-reel
- Nothing else!





Embedding by AT&S

Benefits

- High integration
- High performance
- Very-high-scale production

⇨ Efficient and cost-effective technology

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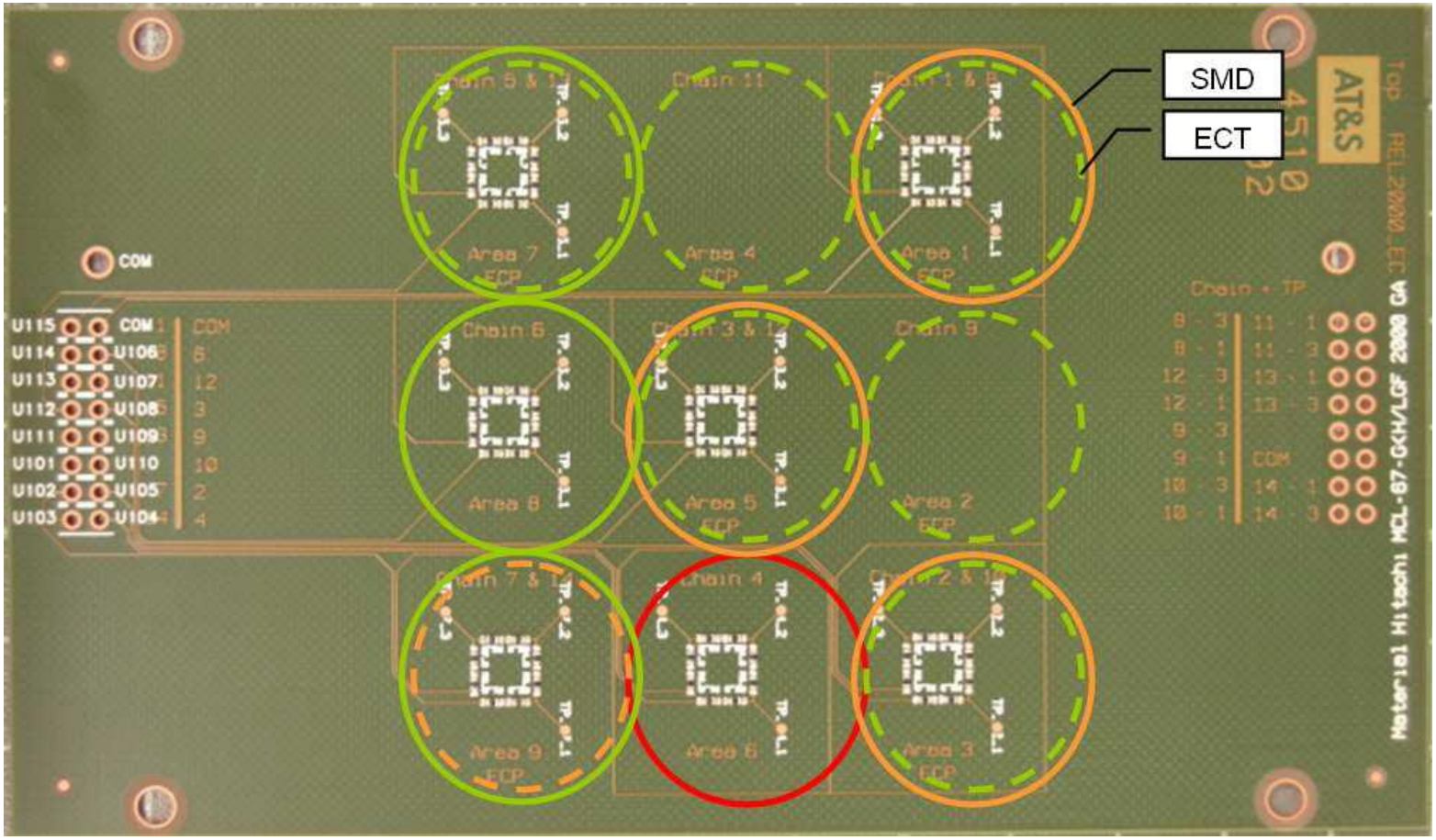
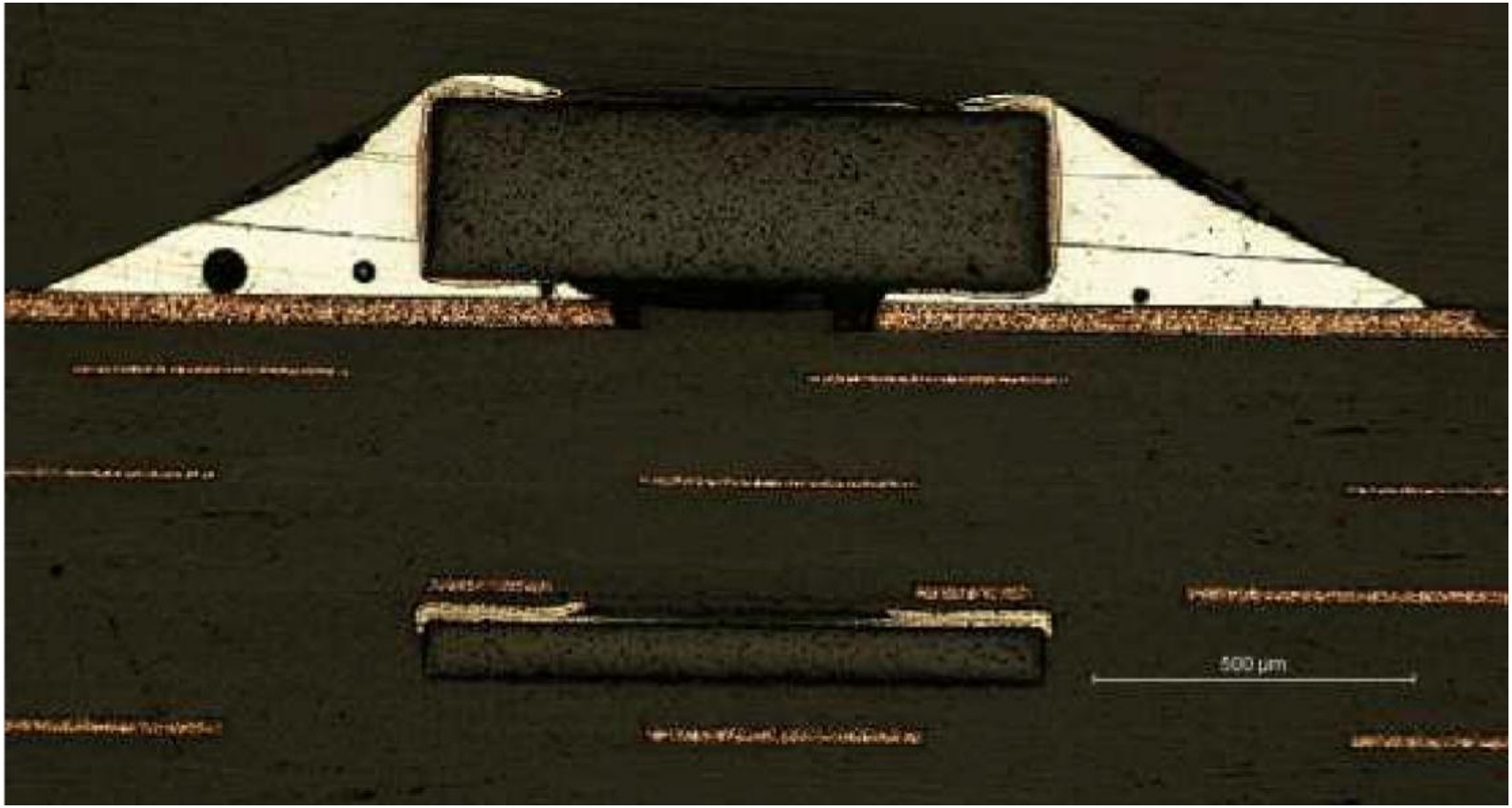
Reliability comparison

Passives



Reliability comparison

Passives



Reliability comparison

Passives

- Drop test (JESD22-B111) @ 1500 g
  - SMT components (126 daisy chains)
  - ⇨ First failure @ 304 drops
  - ⇨ 100-% failure @ 974 drops
  - ECP components (126 daisy chains)
  - ⇨ First and only failure @ 832 drops
  - ⇨ Test end @ 1000 drops

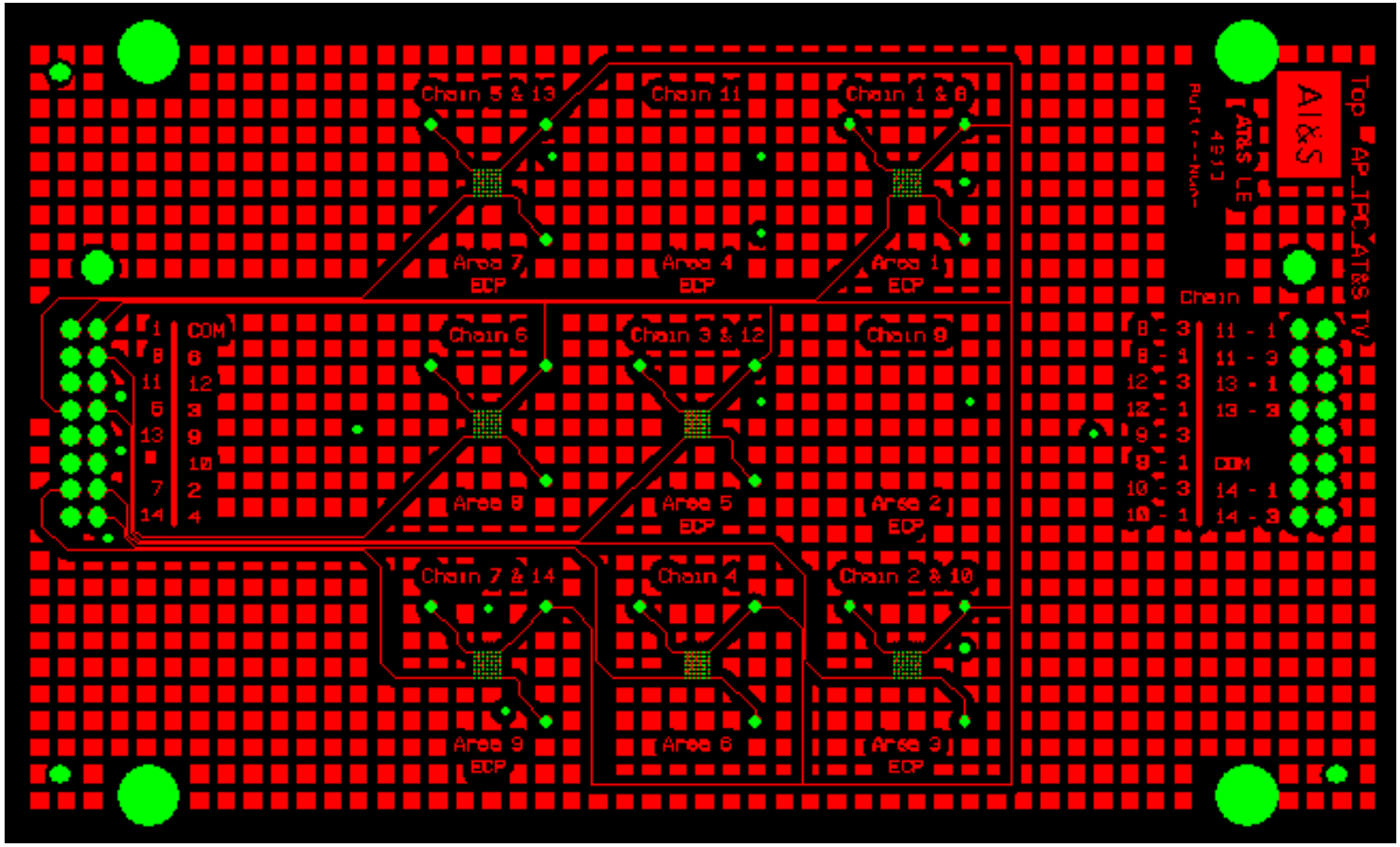
Reliability comparison

Passives

- TCT (JESD22-A104C) @ [-40; +125] degC
  - SMT components (35 daisy chains)
  - ⇨ Zero failure @ 1000 cycles
  - ECP components (35 daisy chains)
  - ⇨ Zero failure @ 1000 cycles

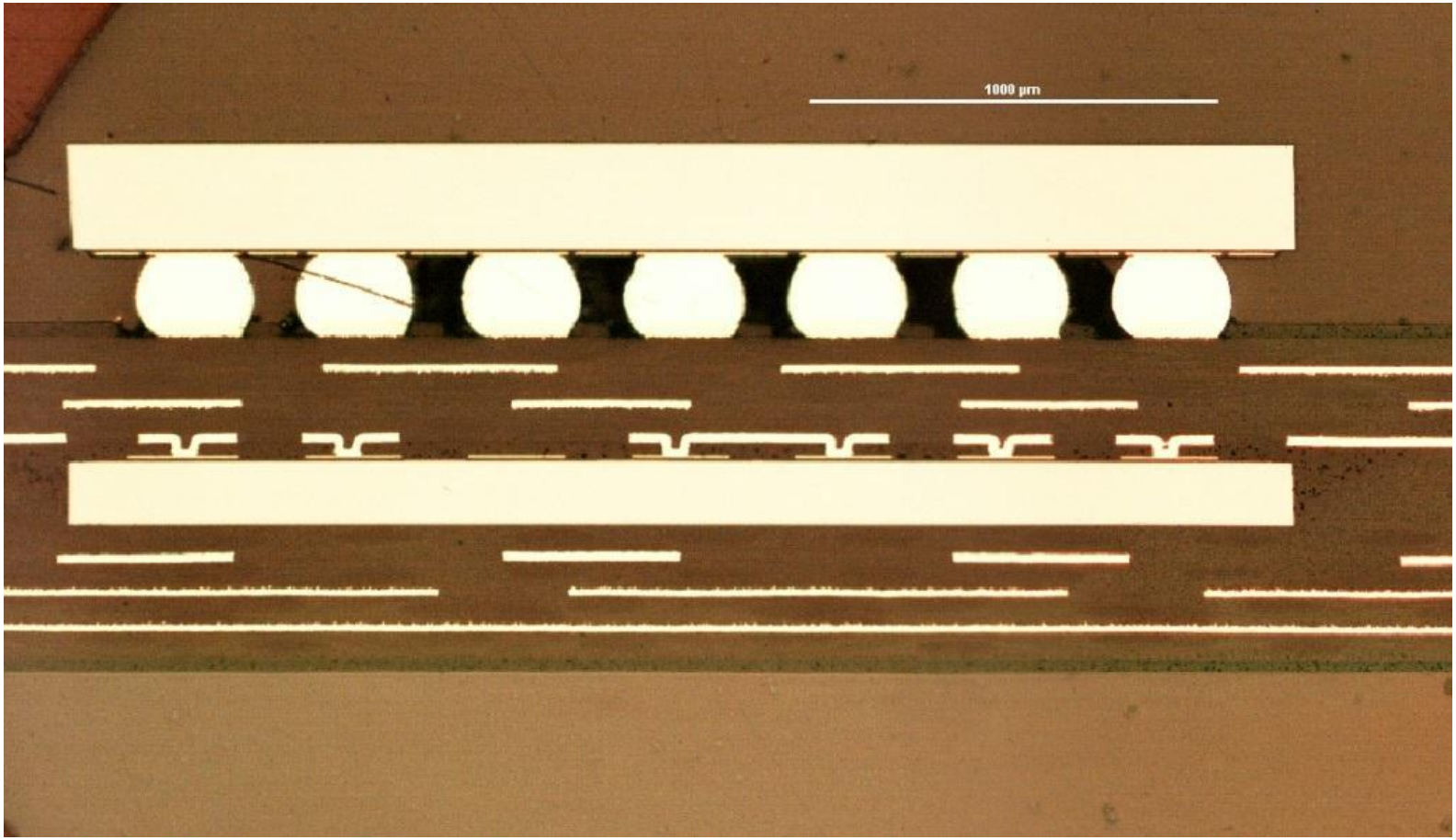
Reliability comparison

Actives



Reliability comparison

Actives



Reliability comparison

Actives

- Drop test (JESD22-B111) @ 1500 g
  - SMT components (70 daisy chains)
  - ⇨ First failure @ 792 drops
  - ⇨ 4 failures @ 1000 drops
  - ECP components (70 daisy chains)
  - ⇨ Zero failure @ 1000 drops

Reliability comparison

Actives

- TCT (JESD22-A104C) @ [-40; +125] degC
  - SMT components (70 daisy chains)
  - ⇨ First failure @ 684 cycles
  - ⇨ 100-% failure @ 999 cycles
  - ECP components (70 daisy chains)
  - ⇨ Zero failure @ 1000 cycles

Reliability comparison

Actives

- Bend test (JEDEC-9702) @ 2 mm/min (28 mm maximum)
  - SMT components (63 daisy chains)
  - ⇨ First and only failure @ 3.71 s
  - ECP components (63 daisy chains)
  - ⇨ Zero failure @ 14 min

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Supply chain

Suppliers

- Actives
  - Cu available from selected foundries
  - RDL available from OSATs
- Passives
  - Resistors available from AVX and Murata
  - Capacitors available from KOA and Panasonic
- IPDs
  - Available from IPDiA , Maxim and STMicroelectronics

Supply chain

Technology complexity (or lack thereof)

- Standard PCB processes
- Standard SMT processes
- Main production facilities in China

⇨ Very quick capacity extension possible

Supply chain

Integration in packaging flow

- Very-high-yield process

⇨ 2L @ 99+ %

- Flexibility of delivery format

⇨ Any size up to 400*550 mm

- Intermediate-testing relevance
  - If QFN replacement
    - ⇨ Only after singulation
  - If SiP
    - ⇨ Do you test after every component placement/interconnection?

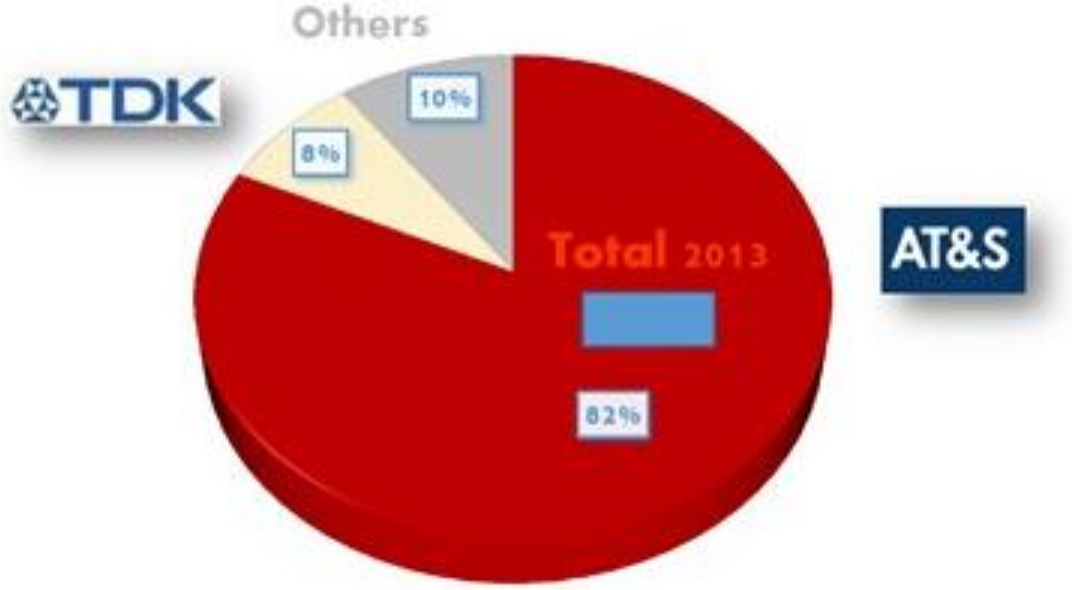
⇨ Seamless integration in standard packaging flow

Supply chain

Partnership

- Agreement with TDK-EPCOS
  - TDK-EPCOS as second source for ECP
  - AT&S as second source for SESUB
  - ⇨ Limiting customer concerns with regards to technology selection/dissemination
  - Co-development of next-generation embedding technology
- Need to encourage ecosystem

⇨ Risk of customer distrust (monopoly)



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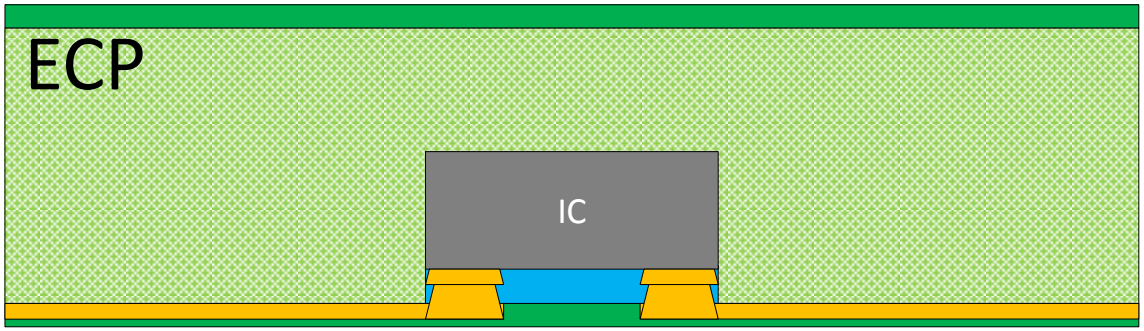
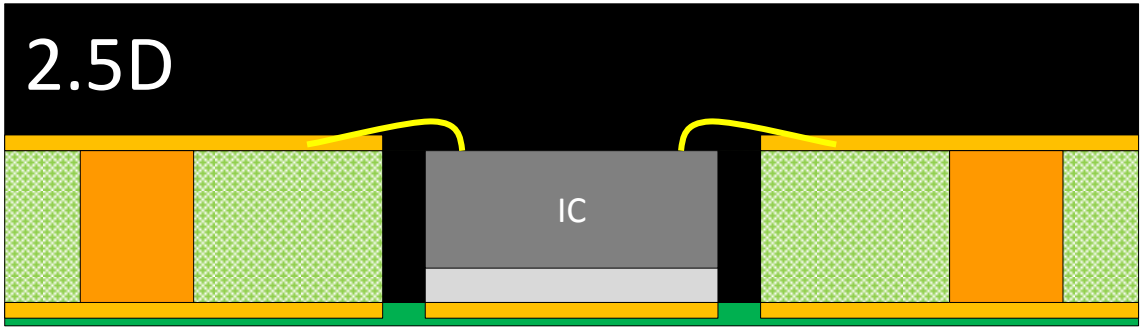
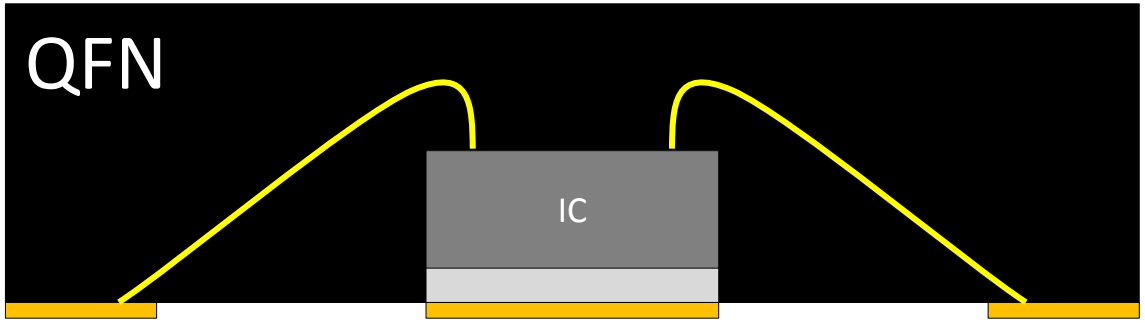
Comparison with QFN

Structure







Comparison with QFN

Characteristics

		ECP	2.5D	QFN
Die size (mm)		2*2		
Package size (mm)		4*4		
Number of I/Os		12		
Die thickness (µm)		150	300	300
Package thickness		300	500	700
Interconnect		Via	WB	WB
Thermal resistance (K/W)	θ_{j-top}	30	94	120
	$\theta_{j-bottom}$	0.7	0.6	0.7
	$\theta_{j-ambient}$	0.7	0.6	0.7
Interconnect inductance (nH)		0.7	0.7	1.0
Cost		+	+	0
Testability		QFN footprint		

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Embedding

- Different variants depending on requirements
  - Embedded layer
  - Partial embedding
  - Full embedding
- Improved performance for limited to neutral cost increase
  - Size reduction
  - Improved thermal resistance
  - Improved electrical characteristics
- Maturing and reliable technology
- Full supply chain in place with second-source options

⇨ What will be the next big application?

Thank you for your attention!

Questions?

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